What is Claimed is:

[c1]   A system for verifying an integrated circuit design comprising:

an I/O controller connected to one or more I/O cores, said I/O cores part of said integrated circuit design;

an external memory mapped test device having a switch for selectively connecting one or more of said I/O cores to corresponding I/O driver models;

a bus for transferring signals between said I/O controller and said switch; and

a test operating system for controlling said switch.

[c2]   The system of claim 1, wherein said external memory mapped test device and said switch are distributed among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models.

[c3]   The system of claim 1, wherein said external memory mapped test device further includes an address register for setting said switch and controlling said I/O driver models.

[c4]   The system of claim 1 wherein said integrated circuit design further includes an embedded processor for running said test operating system.

[c5]   The system of claim 2, wherein each said external memory mapped test device module further includes an address register for setting said portion of said switch and controlling said one I/O driver model.

[c6]   The system of claim 2, wherein said integrated circuit design further includes an embedded processor for running said test operating system.

[c7]   The system of claim 1, wherein said external memory mapped test device and said switch are distributed among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models and further including an additional external memory mapped test device module directly connected to one or more additional I/O driver models, each additional I/O driver model directly

connected to an additional I/O core, each additional I/O core part of said integrated circuit design.

[c8]   A method for verifying an integrated circuit design comprising:

providing an I/O controller connected to one or more I/O cores, said I/O cores part of said integrated circuit design;

providing an external memory mapped test device having a switch for selectively connecting one or more of said I/O cores to corresponding I/O driver models;

providing a bus for transferring signals between said I/O controller and said switch;

providing a test operating system for controlling said switch; and

simulating said integrated circuit design by running a test case on said test operating system.

[c9]   The method of claim 8, further including:

distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models.

[c10]   The method of claim 8, further including:

providing said external memory mapped test with an address register for setting said switch and controlling said I/O driver models.

[c11]   The method of claim 8, further including:

providing an embedded processor in said integrated circuit design for running said test operating system.

[c12]   The method of claim 9, further including:

providing each external memory mapped test device module with an address register for setting said portion of said switch and controlling said one I/O driver model.

[c13]   The method of claim 9 , further including:

providing each integrated circuit design with an embedded processor for

running said test operating system.

[c14]   The method of claim 8, further including:
          distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models: and
          providing an additional external memory mapped test device module directly connected to one or more additional I/O driver models, each additional I/O driver model directly connected to an additional I/O core, each additional I/O core part of said integrated circuit design.

[c15]   A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for verifying an integrated circuit design, said method steps comprising:
          providing an I/O controller connected to one or more I/O cores, said I/O cores part of said integrated circuit design;
          providing an external memory mapped test device having a switch for selectively connecting one or more of said I/O cores to corresponding I/O driver models;
          providing a bus for transferring signals between said I/O controller and said switch; providing a test operating system for controlling said switch; and
          simulating said integrated circuit design by running a test case on said test operating system.

[c16]   The program storage device of claim 15, said method steps further including:
          distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models.

[c17]   The program storage device of claim 15, said method steps further including:
          providing said external memory mapped test with an address register for setting said switch and controlling said I/O driver models.

[c18]   The program storage device of claim 15, said method steps further including:
         providing an embedded processor in said integrated circuit design for
         running said test operating system.

[c19]   The program storage device of claim 16, said method steps further including:
         providing each external memory mapped test device module with an
         address register for setting said portion of said switch and controlling
         said one I/O driver model.

[c20]   The program storage device of claim 16, said method steps further including:
         providing each integrated circuit design further with an embedded
         processor for running said test operating system.